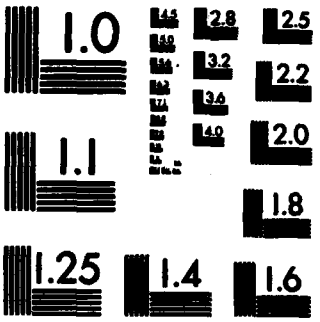
AD-A145 640 FAULT TOLERANT COMPUTING RESEARCH(U) OAKLAND UNIV 1/1
ROCHESTER MI SCHOOL OF ENGINEERING D K PRADHAN SEP 83
AFOSR-TR-84-0841 AFOSR-80-0217

UNCLASSIFIED F/G 9/2 NL



UNCLASSIFIED
SECURITY CLASSIFICATION

AD-A145 640

4

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION
UNCLASSIFIED

RESTRICTIVE MARKINGS

2a. SECURITY CLASSIFICATION AUTHORITY

3. DISTRIBUTION/AVAILABILITY OF REPORT
Approved for public release; distribution unlimited.

2b. DECLASSIFICATION/DOWNGRADING SCHEDULE

4. PERFORMING ORGANIZATION REPORT NUMBER(S)

5. MONITORING ORGANIZATION REPORT NUMBER(S)
AFOSR-TR- 84-0841

6a. NAME OF PERFORMING ORGANIZATION
Oakland University

6b. OFFICE SYMBOL (If applicable)

7a. NAME OF MONITORING ORGANIZATION
Air Force Office of Scientific Research

6c. ADDRESS (City, State, and ZIP Code)
School of Engineering
Rochester MI 48063

7b. ADDRESS (City, State, and ZIP Code)
Directorate of Mathematical & Information Sciences, AFOSR, Bolling AFB DC 20332

8a. NAME OF FUNDING/SPONSORING ORGANIZATION
AFOSR

8b. OFFICE SYMBOL (If applicable)
NM

9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
AFOSR-80-0217

8c. ADDRESS (City, State, and ZIP Code)
Bolling AFB DC 20332

10. SOURCE OF FUNDING NUMBERS

PROGRAM ELEMENT NO.	PROJECT NO.	TASK NO.	WORK UNIT ACCESSION NO.
61102F	2304	A6	

11. TITLE (Include Security Classification)
FAULT TOLERANT COMPUTING RESEARCH

12. PERSONAL AUTHOR(S)
D.K. Pradhan

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM 1/7/80 TO 30/6/83	SEP 83	10

16. SUPPLEMENTARY NOTATION
The author is presently at the Dept of Electrical & Computer Engineering, Univ of Massachusetts, Amherst MA 01003.

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

During this period the principal investigator completed 18 technical papers for the refereed learned journals. Three main topics were investigated: (1) Design of fault tolerant computers using read-only memories as basic building blocks; (2) Design of programmable logic arrays and sequential networks for testability; and (3) Design of fault tolerant multiprocessor network architectures. Some titles of the resulting papers are: "Sequential network design using extra inputs for fault detection", "A class of unidirectional error correcting codes", "A uniform representation of permutation networks used in memory processor interconnections", and "A fault tolerant communication architecture for distributed systems."

DTIC ELECTE SEP 19 1984 S E

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT
☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT. ☐ DTIC USERS

21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL
CPT Brian W. Woodruff

22b. TELEPHONE (Include Area Code)
(202) 767-5027

22c. OFFICE SYMBOL
NM

DD FORM 1473, 84 MAR 83 APR edition may be used until exhausted
All other editions are obsolete

SECURITY CLASSIFICATION OF THIS PAGE
UNCLASSIFIED

DTIC FILE COPY

84 09 18 092

AFOSR-TR- 84-0841

Fault-Tolerant Computing Research*

report to

Air Force Office of Scientific Research

Ref. No: AFOSR 80-0217

1 July 1980 - 30 June 1983

D. K. Pradhan

* Research carried out while the author was at Oakland University, Rochester, Michigan 48057

+ Author's present address: Department of Electrical & Computer Engineering, University of Massachusetts, Amherst, Massachusetts 01003

I. INTRODUCTION

The following reports on research performed under the sponsorship of AFOSR, for a period of approximately three and half years. This research has primarily focused on the following three aspects of fault-tolerant computing.

1.1 Design of fault-tolerant computers using read-only memories (ROMs) as basic building blocks.

1.2 Design of programmable logic arrays (PLA's) and sequential networks for testability

1.3 Design of fault-tolerant multiprocessor network architectures.

During this initial period of the grant, major emphasis was placed on the first two topics; research on the third topic has more recently been initiated and is continuing here at the University of Massachusetts. In this report, we present highlights of these research activities, as well as the pertinent research results.

This report is organized into the following main sections: In Section II, a summary of all important results is given. Following this, in Section III, a list is provided of all associated personnel linked to the research activities. Finally, is a complete listing of publications that resulted from the research supported by the grant.

II. SUMMARY OF RESEARCH RESULTS

This section is divided into three subsections, 2.1, 2.2 and 2.3., which discuss the results that correspond to 1.1, 1.2 and 1.3, above, respectively.

2.1 Initial research was primarily concerned with the development of techniques that will enhance the use of ROM as a basic building block in fault-tolerant computers. The predominant motivation here is that fault-tolerant techniques can, then, more easily be incorporated in ROM-based logic. The following results were formulated:

To begin with, a decomposition technique was proposed that allows for any multiple output function to be decomposed into subfunctions. This was achieved by using Galois switching theory that was developed earlier by the author. This technique provided a new and practical method to decompose a large ROM into an interconnection of smaller ROM's. The effectiveness of our technique was evaluated for specialized arithmetic functions such as multipliers. It was shown that for a large class of functions; decompositions are indeed possible, resulting in a drastic reduction in logic.

Secondly, a new class of codes, specially suited for ROM-based logic, was developed, possessing the following properties:

Error correcting/detecting codes that are effective against both random and unidirectional errors are useful in providing protection against both permanent and transient faults. Therefore, what has been developed is a new error-control strategy. Of particular concern here is when the likelihood of both random and unidirectional errors exists. Transient faults are likely to cause random errors, whereas permanent faults cause either random or unidirectional errors, depending on the nature of the faults. As an example of unidirectional errors, consider a power supply or a stuck-fault in

a serial bus. This can result in changing the received work to all 0 or all 1.

Here, a class of t-error correcting and multiple unidirectional error detecting systematic codes was developed. These codes are significantly more efficient than the earlier codes. The efficiency of these codes approaches the efficiency of the BCH codes, asymptotically. Furthermore, it was shown that these codes can be easily decoded. Also we have developed a generalization of Berger codes over Z_q; these new codes are also shown to be optimal.

These coding techniques have been used to propose certain fault-tolerant ROM-based logic design methods.

2.2 Next, research was carried out in the area of design for testability for programmable logic arrays (PLA's) and sequential networks. PLAs are increasingly replacing the custom logic elements - insofar as the design of a wide variety of digital systems is concerned. The chief advantage of PLA's is their regularity; this results in both simpler designs and fast turn-around time. However, the increasing complexity of PLA circuits has meant that the traditional stuck-at fault model has become inadequate.

Therefore, recently growing attention has been focused on other more complex types of faults. An important class of such faults is that of bridging faults. In fact some of the recent studies have shown that bridging faults (short circuits) are actually the cause of many failures.

Here, the effects of undetectable bridging faults in programmable logic arrays was studied. Furthermore, it was shown that an undetectable bridging fault can invalidate a crosspoint fault test set. A design of PLA's was

also presented in which one can detect all single bridging faults by applying at most (m+2) tests (where m is the number of product lines). The proposed design may require at most two extra inputs.

The design of sequential networks that can facilitate fault detection is becoming an ever-increasing concern. Here, a new fault-detecting design of sequential networks was developed. Specifically, this design allows for the use of any arbitrary number of inputs. This, therefore, can be interpreted as a generalization of scan-in/scan-out design. The new design was evaluated in the framework of checking sequences; it was shown to be optimal. Additionally, the new design was demonstrated to be cost effective from the point of view of hardware design cost. Specifically, only a small number of extra gates are required to incorporate the testability features.

2.3 The later phase of the research has focused on one of the most vital and important areas of fault-tolerant computing research today - that is, how fault-tolerance can be incorporated into multiprocessor network architectures. This particular problem has taken on a new dimension in the context of VLSI which, for the first time, makes it possible to interconnect a large number of computing elements together so as to form an integrated system.

The author has developed several new fault-tolerant interconnection architectures that allow fault-tolerance to be incorporated as an integral part of the design. Also what is being developed is a systematic design methodology that can incorporate various fault-tolerance features directly into such network systems. A goal of this research, then , is to develop a sound framework through which pertinent design considerations can be expressed quantitatively; thus, the basis for exploring newer fault-tolerant

architectures is provided. This is formulated by using the system interconnection structure as the fundamental design component for the achievement of a wide variety of fault-tolerant objectives.

Interconnection structure design for closely-coupled integrated multi-processor systems differs in a significant way from that used in other computer networks. This is chiefly due to the factors of the speed, size and computational environment constraints that are unique to these systems. Specifically, it is becoming increasingly recognized that for a large multi-processor system, the network topology must possess the properties of low interconnection complexity, simple routing, dynamic reconfigurability, fault-tolerance, and the like.

All of these requirements can only be achieved if the system interconnection architecture is designed using a systematic design methodology that incorporates these requirements as an integral part of the design (and not an an 'after thought'). For example, in order to simplify routing overhead, the network must be able to support algorithmic-based routing, so that the nodes can be relieved of having to maintain routing tables, directories, etc., which can be unwieldy and costly for large systems. Dynamic reconfigurability requires that the system interconnection efficiently admit different logical structures, such as binary tree, linear array, etc.

Finally, fault-tolerance should be incorporated at the system interconnection level. Thus, graceful degradation can be provided for so that full connectivity among all of the surviving elements is maintained, in spite of fault-induced changes.

In implementing fault-tolerance, the effects of link, node and subsystem faults must all be taken into account (where a subsystem may contain a cluster of nodes). Importantly, the effectiveness of any fault-tolerant

technique depends greatly on the effectiveness of the testing and diagnosis capabilities provided to detect and locate the faulty link(s), node(s), and subsystem(s). The following elaborates more fully on these considerations.

Another area of research is the development of architectures, built by interconnecting a large number of processing elements on a single chip or wafer. Two different important problems, related to such VLSI processor arrays are the focus of this research; they are fault-tolerance, and the development of techniques that better utilize the inherent computational capabilities of these arrays.

Fault-tolerance in these VLSI processor arrays is of real practical significance; it provides for much-needed reliability improvement, as well as for yield enchancement. Therefore, what is being studied, first, is to identify those underlying concepts and relationships of fault-tolerance at work in these arrays. These precepts are useful to then formulate certain techniques that will incorporate fault-tolerance integrally into the design. Also being developed are models that evaluate how yield enhancement may be achieved by certain new fault-tolerant techniques.

Secondly, what has been developed is a novel approach that uses these arrays for general computation, an approach which is based on the mapping of certain data flow graphs directly onto these arrays. The overall effectiveness of the approach is augmented by indicated research developing detailed architectural supports for implementation and optimization of the design for cost-performance improvements.

III. **PERSONNEL** (supported in part or whole by the grant)

D. K. Pradhan (Principal Investigator)
B. Bose
A. Itai
K. Son *
A. Cesnak *

* Currently working on the project, supported temporarily from state funds

IV. PUBLICATIONS (supported directly by AFOSR 80-0217).

TEXT BOOK

Fault-Tolerant Computing: Theory and Techniques, Prentice-Hall, Inc., (Forthcoming, 1983).

IN JOURNAL:

1. "Sequential Network Design Using Extra Inputs for Fault Detection," IEEE Transactions on Computers, March 1983.

2. "Synthesis of Multi-commodity Flow Problems," Networks, (to appear).

3. "A fault-Tolerant Distributed Processor Communication Architecture," IEEE Transactions on Computers, September 1982.

4. "A Class of Unidirectional error correcting codes," IEEE Transactions on Computers, June 1982.

5. "A Uniform Representation of Permutation Networks Used in Memory-Processor Interconnection," IEEE Transactions on Computers, Special Issue on Parallel Processing, September, 1980, (with K. L. Kodandapani), pp. 777-791.

6. "A New Class of Error Correcting-Detecting Codes for Fault-Tolerant Computer Applications," IEEE Transactions on Computers, Vol. C-29, No. 6, pp. 471-481, June, 1980.

7. "Error-Correcting Codes and Self-Checking Circuits," IEEE Computer, Vol. 13, Number 3, pp. 27-38, March, 1980. (with J. J. Stiffler).

8. "Undetectability of Bridging Faults and Validity of Stuck-at Fault Test Sets,: IEEE Transactions on Computers, Vol. C-29, No. 1, (with K. L. Kodandapani) pp. 55-59, January, 1980.

9. "Partitionability and Diagnosability of a Class of Multiprocessor Network Architectures," Proc of International Conference on Distributed Processing, Miami, Florida, October, 1982.

10. "Interconnection Topologies for Fault-Tolerant Parallel and Distributed Architectures," Proc. of 10th International Conference on Parallel Processing, pp. 238-242, August 1981.

11. "Fault-Diagnosis of Parallel Processor Interconnection Networks," Proc. Eleventh Annual International Symposium on Fault-Tolerant Computing, pp. 209-212, June 1981.

12. "A Fault-Tolerant Communication Architecture for Distributed Systems," Proc. Eleventh International Conference on Parallel Processing, pp. 214-220, June 1981.

13. "A Solution to Load-Balancing and Fault Recovery in Distributed Systems," Symposium on Reliability in Distributed Software and Database Systems, July 1981.

14. "A Fault-Diagnosis Technique for Closed Flow Networks," Proc. of 1980 Symposium on Fault-Tolerant Computing, Kyoto, Japan, October 1980.

15. "An Easily Testable Design of PLAs," Cherry Hill Test Conference, Philadelphia, November 1980. (Reprinted in IEEE Tutorial on Testing by Rex Rice).

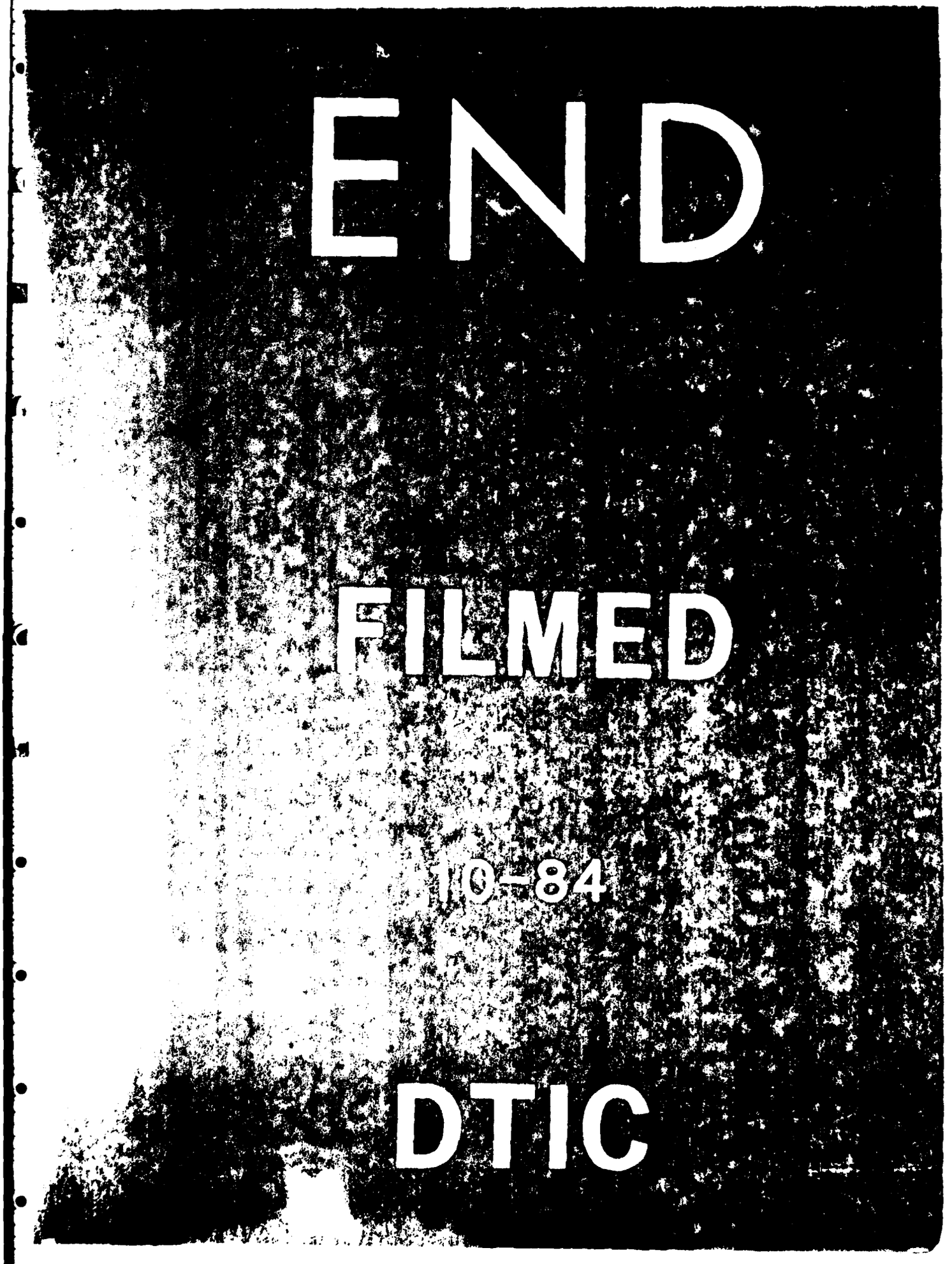
16. "A Generalization of Shuffle-Exchange Networks," Proc. of Fourteenth Annual Conference on Information Sciences and Systems, Princeton, New Jersey, March, 1980.

17. "A Framework for the Study of Permutations and Applications to Memory Processor Interconnection Networks;" Proc., 1979 International Conference on Parallel Processing, pp. 148-158, August, 1979. (with K. L. Kodandapani).

18. "Fault-Tolerant Network Architectures for Multiprocessors and VLSI Based Systems", FTCS-13, to appear.

V CONCLUDING REMARKS

The accomplished research has been able to cover a broad spectrum of important areas in fault-tolerant computing. Also continuing actively is research in the area of fault-tolerant network architectures in the area of multiprocessors and VLSI-based systems.


END
FILMED
10-84
DTIC